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Importance of active layer positioning on gate electrode in organic thin-film transistors

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ABSTRACT
We describe the importance of active layer positioning for a gate electrode in organic thin-film transistors (TFTs). For this study, we utilizea numerical simulation based on 2-D Atlas, which is a two-dimensional technology computer aided design (so called 2D TCAD) software tool created by Silvaco. Variation in the electrical characteristics of pentacene TFTs is systematically explored by changing the mismatch length (L_M) between the active layer and gate electrode in the bottom-gate top-contact configuration. It is found that as the L_M increases, the electrical performance of pentacene TFTs is exponentially degraded in terms of drain current on/off characteristics. In particular, we explain this phenomenon by examining variations in charge distribution and gate electric field in the TFT channel region byincreasing the L_M.

KEYWORDS
Channel; electric field; mismatch length; organic thin-film transistor

1. Introduction

Organic thin-film transistors (TFTs) have attracted considerable attention due to their features of mechanical flexibility and low-temperature process, and their applicability to next-generation displays and sensors [1–3]. Thus, over the last decades, a large amount of research has been conducted to find various materials and optimize various processes to improve performance. In particular, organic TFTs are fabricated by the layer-by-layer deposition method, in which thin-films of electronic materials, including organic semiconductors, are stacked using various techniques such as vacuum or solution processes. Therefore, alignment among thin films is a critical factor affecting the electrical properties of a device. In particular, alignment necessitates that the electric field is properly distributed. Because a conducting channel is formed in an active layer by the gate field, precise alignment between the active layer and gate electrode is necessary [4]. However, the effect of mismatch between the active layer and gate electrode on device properties has not yet been fully examined in terms of carrier distribution.

In this study, we investigate the importance of active layer positioning for gate electrodes inorganic TFTs through numerical simulation using ATLAS, created by Silvaco. We analyzed the output and transfer of a TFT' selectrical characteristics with increasing mismatch length

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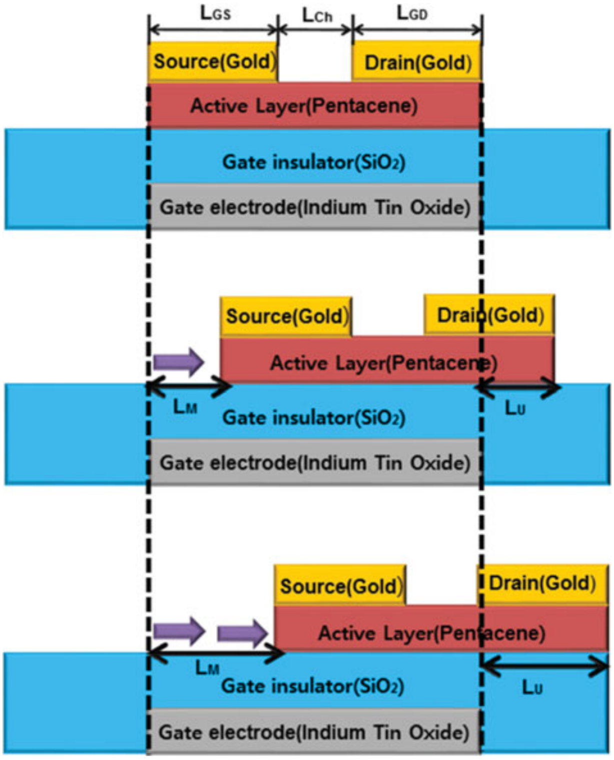

Figure 1. Schematic illustration of the simulated organic TFTs. Channel overlap length, source-to-gate electrode overlap length, drain-to-gate electrode overlap length, non-overlap length, and mismatch length are varied from 0 μm, 20 μm, 40 μm, 60 μm, and 70 μm.

(L_M) between the active layer and gate electrode. To explain the variation, we simulated the hole concentration and gate electric field at the interface between the active layer and gate insulator.

2. Simulation methodology

Figure 1 illustrates the structure of an organic TFT device with a top-contact, bottom-gate staggered structure [1]; the channel length is L_{Ch}, the source-to-gate electrode overlap length is denoted by L_{GS}, the drain-to-gate electrode overlap length is denoted by L_{GD}, the gate-active layer mismatch length is L_M, the gate-active layer un-overlap length is L_U, and the L_U upper region is the non-overlap region. The gate and source/drain electrodes are made of indium tin oxide (ITO) and gold, respectively. The lengths of the gate and source/drain are 70 μm and 10 μm, respectively. The thickness of those electrodes is 50 μm [6]. The work functions of ITO and gold are 4.7 and 5.1 eV, respectively. The gate insulator is made of 50 nm thick SiO_2. The active layer characteristics are based on pentacene, which is a small-molecule classical substance that actsas a p-type organic semiconductor. The parameters are taken from previous works [7–9]. In this study, the active layer is considered to be a p-doped semiconductor with a $5 \cdot 10^{12}$ cm^{-3} concentration [10]. The parameters of the materials used are shown in Table 1. For the numerical simulation, we used a numerical simulation based on 2-D Atlas, which is a 2D TCAD software tool created by Silvaco [11]. The electrical characteristics of the device were estimated for a particular bias condition by solving the Poisson and continuity partial

Table 1. Parameters of organic thin-film transistor material properties.

Region	Gate	Gate insulator	Source/Drain	Organic semiconductor			
Material	ITO	SiO_2	Gold	Pentacene			
Parameter	Work function	Relative permittivity	Work function	Bandgap	Electron affinity	Relative permittivity	Effective density of state of conduction (Nc)/valence band (Nv)
Value	4.7 eV	3.9	5.1 eV	2.2 eV	2.8 eV	3.9	$2\cdot10^{21}$ cm^{-3}

differential equations [12]:

$$\varepsilon\nabla^2\psi = -pq,\ \frac{\partial p}{\partial t} = \frac{1}{q}\nabla\cdot J_p + G_p - R_p,\ \text{and}\ J_p = qp\mu_pF + qD_p\nabla p,$$

where ε is the relative permittivity, ψ is the potential, p is the local hole density, q is the fundamental electronic charge, J_p is the current density, G_p is the charge generation rate, R_p is the charge recombination rate, μ_p is the hole mobility, F is the electric field, and D_p is the hole diffusion coefficient.

3. Results and discussion

Figure 2 shows the output characteristics of the simulated organic TFTs for various L_M between the active layer and gate electrode; 0 µm, 20 µm, 40 µm, 60 µm, and 70 µm. The output characteristics were measured by sweepingthe drain voltage (off to on) from 0 V to −40 V, at −10 V increments of gate voltage from 0 V to −40 V. Figure 2(f) presents the variation insaturation drain current characteristics at gate and drain voltages of −40 V, according to L_M, which ranges from 0 µm to 70 µm. After an L_M of 10 µm, the saturation behavior of the organic TFTs disappears and the output characteristic deteriorates, in terms of current magnitude, with increasing L_M. In particular, the drain current magnitude begins to decrease exponentially after an L_M of 10 µm. The exponential decrease in drain current is presumably associated with the vertical mismatch between the TFT channel region and the gate electrode. Note that the mismatch between the TFT channel region and gate electrode occurs after an L_M of 10 µm, because L_{GD} is 10 µm.

Figure 3 shows the transfer characteristics of the simulate dorganic TFTs for various L_M between the active layer and gate electrode; 0 µm, 20 µm, 40 µm, 60 µm, and 70 µm. The transfer characteristics were measured by sweeping the gate voltage (off to on) from 10 V to −40 V, at drain voltage of −40 V. As the L_M increases, it was shown that performance parameters, including the on current, off current, subthreshold swing (SS), and transconductance, degraded; the on current decreased, the off current increased, the SS increased, and the transconductance decreased. In other words, as the L_M increased, the performance of theorganic TFTs deteriorated in terms of transfer characteristics. Figures 2 and 3 show that the L_M is closely related to the output and performance of theorganic TFTs. Because TFTs are field-effect transistors, they are driven by an electric field. However, the gate electric field in the active layer non-overlap region is exponentially reduced with increasing the L_M and L_U. Conse quently, the channelis not appropriately formed in the non-overlap region. The reason for this is shown in Fig. 4.

Figure 4 shows the hole concentration in the active layer according to the L_M. Hole concentration distribution in organic TFTs for gate voltage = drain voltage = −40 V is shown; color coded hole concentration values are represented by a continuous distribution from a

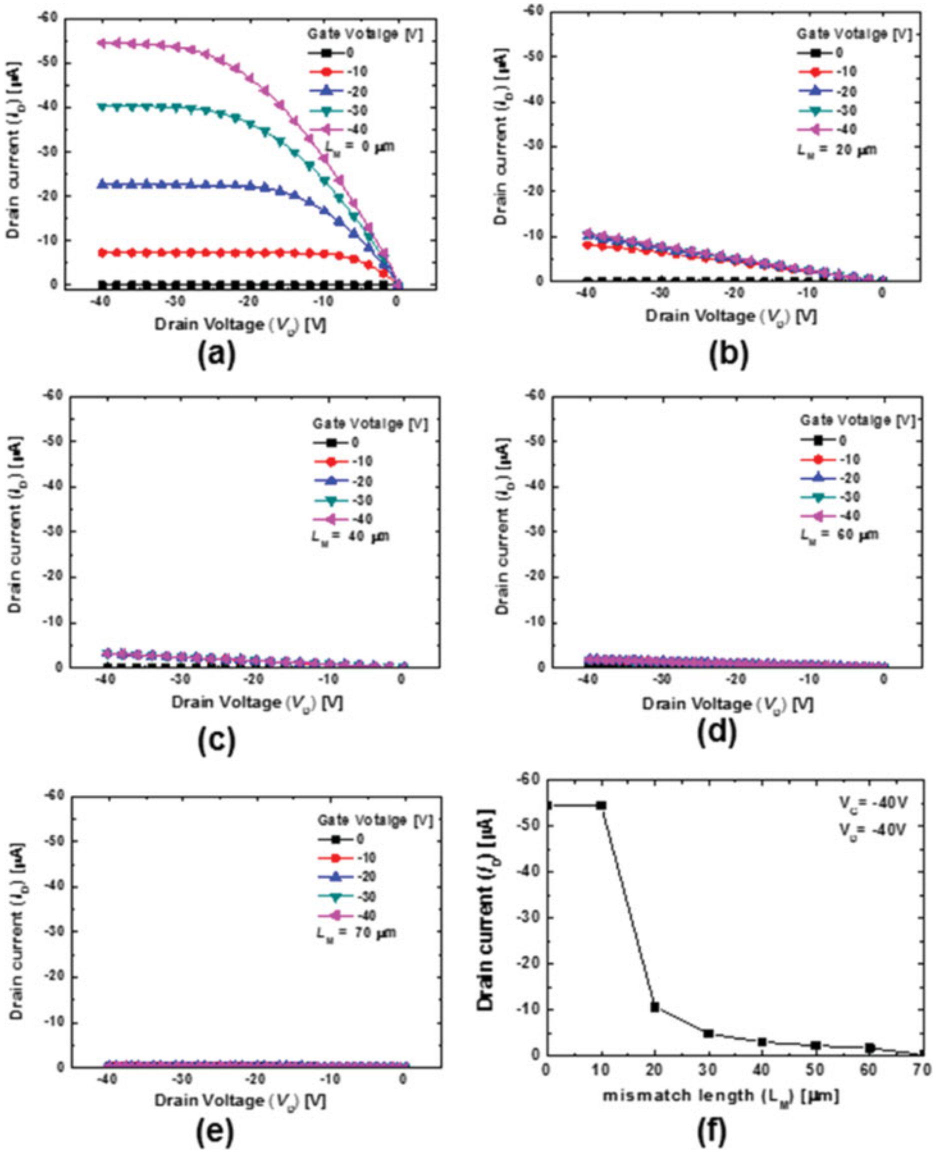

Figure 2. Output characteristics (drain current versus drain voltage) of simulated organic TFTs for various L_M between the gate electrode and active layer; drain voltage (off to on) is swept from 0 V to −40 V, at −10 V increments of gate voltage from 0 V to −40 V. (a) 0 µm, (b) 20 µm, (c) 40 µm, (d) 60 µm, (e) 70 µm, (f) saturation drain current characteristics (drain current versus mismatch length (a)– (e)); gate voltage = drain voltage = −40 V at L_M of 0 µm, 20 µm, 40 µm, 60 µm, and 70 µm.

maximum 10^{19} to a minimum of 0, from red to purple. S denotes the source. D denotes the drain. We consider the relatively reddish region near the interface between the active layer and gate insulator as the TFT channel region. Note that the region of high hole concentration is the organic TFT channel in the active layer. It is shown thatas the L_M increases, non-overlap region hole concentration exponentially reduces. Thus, the channel is not properly formed in the non-overlap region. Therefore, as the L_M increases, the electric field does not form a channel in the non-overlap region. Thus, no current flows. Figure 4(a) also shows that the channel

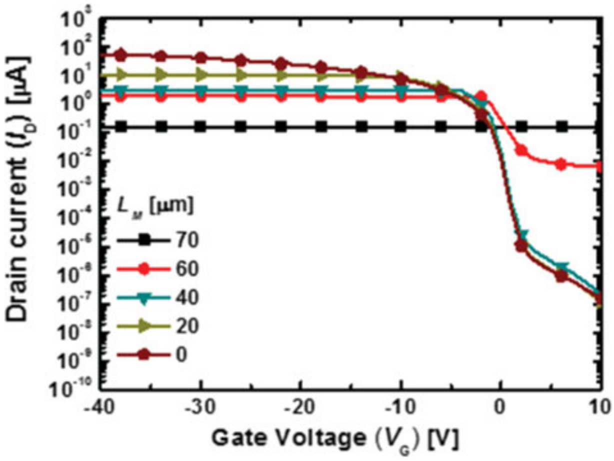

Figure 3. Transfer characteristics (drain current versus gate voltage) of simulated organic TFTs for various L_M between the gate electrode and active layer; gate voltage (off to on) is swept from 10 V to −40 V; drain voltage = −40 V.LM of 0 μm, 20 μm, 40 μm, 60 μm, and 70 μm.

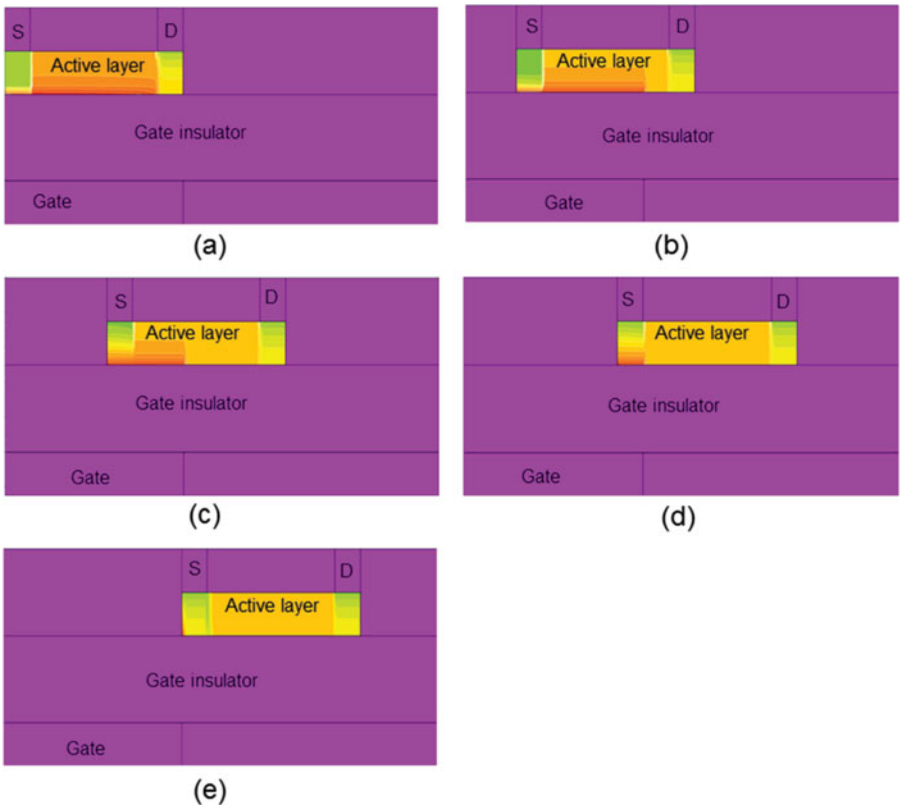

Figure 4. Hole concentration distribution in organic TFTs for gate voltage = drain voltage = −40 V; color-coded hole concentration values; represented by a continuous distribution from a maximum of 10^{19} to a minimum of 0 from red to purple, respectively. L_M is varied (a) 0 μm, (b) 20 μm, (c) 40 μm, (d) 60 μm, and (e) 70 μm.

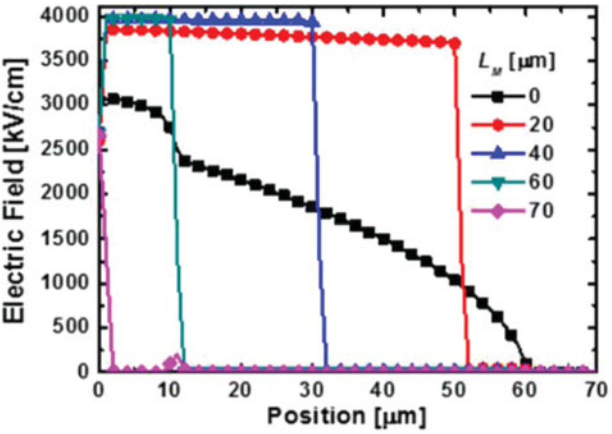

Figure 5. Gate electric field versus active layer positioning in a channel of simulated organic TFTs for various LM; gate voltage = drain voltage = −40 V.

formation range isat the bottom active layer between the source and drain, which can be confirmed by the fact that the channel is between 10 and 60 of the active layer. This might be the reason for the exponentially decreasing saturation drain current in Fig. 2. Therefore, the reduction of the output characteristics leads to an exponential reduction in the gate electric field in the non-overlap region as the L_M becomes larger. Further, it is shown that as the L_M becomes longer, the gate electric field is lost and the field-effect transistor does not operate. As a result, the on current decreases, the off current increases, the SS increases, and the transconductance decreases. Therefore, as the L_M increases, output and transfer characteristics dramatically decrease. The data for the dramatically reduced electric field are shown in Fig. 5.

To explain the variation in hole concentration shown in Fig. 4, gate electric field distribution within the TFT channel region according to L_M was examined. The results are displayed in Fig. 5. Figure 5 was obtained when the bias of gate voltage was −40 V and drain voltage was −40 V. Figures 5 shows that as the L_M increases, the gate electric field, which is a vertical electric field, is not properly applied to the non-overlap region, and only a certain portion of the channel is formed, because the gate electric field is only applied to a specific portion. This indicated that the L_M has a critical factor affecting gate electric field from inside the device. Thus, as the L_M increases, the performance of the device degrades due to the fact that the electric field inside the device is not uniformly affected and the channel is partially formed. In other words, we findthat the alignment of the active layer and gate electrode is very important to optimize device electrical properties.

4. Conclusions

We investigated the property of the device according to the mismatch between the active layer and the gate electrode, and the channel and electric field, based on numerical device simulation. It was confirmed that the device performance decreased exponentially with increasing L_M. Because organic TFTs are field-effect transistors, if L_M between the gate and active layer becomes large, the electric field is dramatically reduced and the channel is only partially formed. Thus, the carriers are injected but not extracted, and the performance of the device is deteriorated. If the device principle isthat of field-effect transistors, the performance of the longer L_M device is dramatically degraded although the material, structure, and process conditions are significantly improved. Therefore, alignment between the active layer and the gate of the device is very important.

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